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10/800,861	03/16/2004	Hiroki Nakamura	250442US2	1575

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EXAMINER	
SEMENENKO, YURIY	

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
06/03/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/800,861	NAKAMURA, HIROKI	
	Examiner	Art Unit	
	YURIY SEMENENKO	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30,31 and 33-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30,31 and 33-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendment filed on 02/27/2008 has been entered.
Claims 30, 31, 33-38 are now pending in the application.

Claims

2. The objection to the claim 35 has been withdrawn.

Claim Rejections - 35 USC § 112

3. The rejections to the claims 31 and 33 have been withdrawn.

Claim Objections

4. Claim 33 is objected to because of the following informalities:
"the first metal diffusion-preventing layer and the second metal diffusion-preventing layer" lack antecedent basis.
Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the

invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 37 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (US 6791112) hereinafter Yamazaki.

As to claim 37: Yamazaki discloses in Fig. 1A a thin-film transistor comprising: a source region 105 and a drain region 106 which are provided with an interval on an insulating substrate 101 (glass- column 4, lines 8-14); a gate insulator layer 112 which is provided over the interval between the source region 105 and the drain region 106; a gate electrode 115 which is provided on the gate insulator layer 112; and a source electrode 120 and a drain electrode 121 which are provided on the source region 105 and the drain region 106, respectively, wherein the gate electrode Fig. 17C comprises: a first copper diffusion-preventing layer 1701(silicon nitride -column 19, lines 7-16) formed on the gate insulator layer 112; a copper layer 1707 (column 18, lines 65-67 and column 4, lines 55-61) formed on the first copper diffusion-preventing layer 1701; and a second copper diffusion-preventing layer 1705 (silicon nitride -column 19, lines 7-16) covering the exposed surface including the side, upper and lower surfaces of the multilayered structure having the copper layer and the first copper diffusion-preventing layer, and wherein the copper layer is surrounded by the fist copper diffusion-preventing layer and the second copper diffusion-preventing layer, and has a forward tapered cross section Fig. 18B and (column 20, lines 14-17).

As to claim 38: Yamazaki discloses the thin-film transistor substantially as claimed claim 37, wherein the insulating substrate 101, Fig. 1A is formed of one of glass, a quartz glass, ceramics, and a resin material (glass- column 4, lines 8-14).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 30, 31, 33 - 35 and 36 are rejected under 35U.S.C. 103(a) as being unpatentable over Yamazaki in view of Ueno et al. (PGPub. No: 2003/0008075) hereinafter Ueno.

As to claim 30: Yamazaki discloses in Fig. 1A a thin-film transistor comprising: a source region 105 and a drain region 106 which are provided with an interval on an insulating substrate 101(glass- column 4, lines 8-14); a gate insulator layer 112 which is provided over the interval between the source region 105 and the drain region 106; a gate electrode 115 which is provided on the gate insulator layer 112; and a source electrode 120 and a drain electrode 121 which are provided on the source region 105 and the drain region 106, respectively, wherein the gate electrode Fig. 17C comprises: a first copper diffusion-preventing layer 1701 (silicon nitride -column 19, lines 7-16) formed on the gate insulator layer 112; a copper layer 1707 formed; and a second copper diffusion-preventing layer 1705 (silicon nitride -column 19, lines 7-16) covering the

exposed surface including the side, upper and lower surfaces of the multilayered structure having the copper layer, and wherein the copper layer is surrounded by the first copper diffusion- preventing layer and the second copper diffusion-preventing layer, and have a forward tapered cross section, Fig. 18B and (column 20, lines 14-17),

except Yamazaki does not explicitly teach a copper seed layer formed on the first copper diffusion-preventing layer.

Ueno discloses in the "Background of the invention" section, [0006] at the time the invention was made, it was well know to use a copper seed layer 17, Fig. 1, formed on the first diffusion-preventing layer 15; and a metal wiring layer 11 formed on the copper seed layer 17 [0029].

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Yamazaki to include in his invention that a metal seed layer formed on the first metal diffusion-preventing layer because Ueno teaches that a Cu seed layer or the like as a conductive layer is required [0006].

As to claim 31: Yamazaki, as modified by the teachinf of Ueno, discloses the thin-film transistor having all of the claimed features as discussed above with respect claim 30, wherein the source electrode 122, Fig. 1A and the drain electrode 121. Although Yamazaki does not explicitly teach the source electrode and the drain electrode comprises: a third copper diffusion-preventing layer formed on the source region and the drain region; a copper wiring layer formed on the third copper diffusion-preventing layer; and a fourth copper diffusion-preventing layer formed to surround the copper wiring layer, this is just repeating claim 30 for the gate electrode and so it is old and well known how to use it. Yamazaki also teaches that such structure permit variations (column 26, lines 8-10). Yamazaki teach identical structure for the gate electrode Fig. 17C comprising: a third metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) formed on the source region 110 and the drain region 109; a copper wiring layer 117 formed on the third metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16); and a fourth metal diffusion-preventing layer formed to surround the copper wiring layer 117.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Yamazaki to include in his invention that the source electrode and the drain electrode comprises: a third copper diffusion-preventing layer formed on the source region and the drain region; a copper wiring layer formed on the third copper diffusion-preventing layer; and a fourth copper diffusion-preventing layer formed to surround the copper wiring layer, because Ueno teaches a Cu seed layer or the like as a conductive layer is required [0006].

As to claim 33: Yamazaki, as modified, discloses the thin-film transistor having all of the claimed features as discussed above with respect claim 31, wherein a plurality of the thin-film transistors 500, 506, Fig. 4 are arranged to form a matrix Fig. 4, and the thin-film transistors have scanning lines 402 connected to the gate electrodes of the thin-film transistors 500, 506, and signal lines 403 connected to one of the source electrodes and the drain electrodes of the thin-film transistors, the signal lines being provided such that they are surrounded by the first metal diffusion-preventing layer (silicon nitride - column 19, lines 7-16) and the second metal diffusion-preventing layer; wherein the gate electrode, the source electrode, and the drain electrode each has wiring connected thereto (column 20, Embodiment 11) and metal diffusion-preventing layer (column 20, lines 47-51); a metal wiring layer of forward tapered cross section (Fig. 18B and (column 20, lines 14-17), which is connects one end thereof to any one of the gate electrode, the source electrode (column 26, lines 8-24).
Although Yamazaki does not explicitly teach film transistors, the signal lines being provided such that they are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer, this is just repeating claim 30 for wiring layer and so it is old and well known how to use it. Yamazaki also teaches that such structure permit variations (column 26, lines 8-10).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Yamazaki to include in his invention that the signal lines being provided such that they are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer, because Ueno teaches that

a Cu seed layer or the like as a conductive layer is required [0006].

As to claim 34: Yamazaki, as modified by the teaching of Ueno, discloses the thin-film transistor having all of the claimed features as discussed above with respect claim 30, wherein the insulating substrate 101, Fig. 1A is formed of one of glass, a quartz glass, ceramics, and a resin material (glass- column 4, lines 8-14).

As to claim 35: Yamazaki discloses in Fig. 1A a thin-film transistor comprising: a source region 105 and a drain region 106 which are provided with an interval on an insulating substrate 101(glass- column 4, lines 8-14); a gate insulator layer 112 which is provided over the interval between the source region 105 and the drain region 106; a gate electrode 115 which is provided on the gate insulator layer 112; and a source electrode 120 and a drain electrode 121 which are provided on the source region 105 and the drain region 106, respectively, wherein the gate electrode Fig. 17C comprises: a first copper diffusion-preventing layer 1701 (silicon nitride -column 19, lines 7-16) formed on the gate insulator layer 112; a copper layer 1707 having a forward tapered cross section, Fig. 18B and (column 20, lines 14-17); and a second copper diffusion-preventing layer (silicon nitride -column 19, lines 7-16) covering the exposed surface including the side, upper and lower surfaces of the multilayered structure having the copper layer, and wherein the copper layer is surrounded by the first copper diffusion-preventing layer and the second copper diffusion-preventing layer,

except Yamazaki does not explicitly teach a copper seed layer formed on the first copper diffusion-preventing layer.

Ueno discloses in the "Background of the invention" section, at the time the invention was made, it was well know to use a metal seed layer 17, Fig. 1 and [0006] formed on the first diffusion-preventing layer 15; and a metal wiring layer 11 formed on the copper seed layer 17 [0029].

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Yamazaki to include in his invention that a metal seed layer

formed on the first metal diffusion-preventing layer because Ueno teaches that a Cu seed layer or the like as a conductive layer is required [0006].

As to claim 36: Yamazaki, as modified by the teaching of Ueno, discloses the thin-film transistor having all of the claimed features as discussed above with respect claim 35, wherein the insulating substrate 101, Fig. 1A is formed of one of glass, a quartz glass, ceramics, and a resin material (glass- column 4, lines 8-14).

Response to Arguments

7. Applicant's arguments filed on 03/26/2007 are considered and acknowledged but are moot in view of the new ground(s) of rejection. Nevertheless, the Examiner points out, in response to applicant's arguments against the Yamazaki 's reference, that "[a]lthough Yamazaki et al. describes using the nitride silicon film from preventing copper from diffusing, it does not teach or suggest where or how it is used" , since the Applicant claims product in claim 37, it is not appropriate to argue about process limitations.

Examiner notes that the question "where or how it is used " are process limitations in product claims. Such process limitations define the claimed invention over the prior art only to the degree that they define the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985). Yamazaki teaches structure which is identical to structure claimed by the Applicant in claim 37, namely, a first copper diffusion-preventing layer 1701(silicon nitride -column 19, lines 7-16) formed on the gate insulator layer 112; a copper layer 1707 (column 18, lines 65-67 and column 4, lines 55-61) formed on the first copper diffusion-preventing layer 1701; and a second copper diffusion-preventing layer 1705 (silicon nitride -column 19, lines 7-16) covering the exposed surface including the side, upper and lower surfaces of the multilayered structure having the copper layer and the first copper diffusion-preventing layer, and

wherein the copper layer is surrounded by the fist copper diffusion-preventing layer and the second copper diffusion-preventing layer, and has a forward tapered cross section Fig. 18B and (column 20, lines 14-17).

The Applicant argues "there is no reason to combine the teachings of Yamazaki et al. with Ueno et al, other than by using Applicant's invention as a template for modifying the claims in a hindsight reconstruction of Applicant's invention." Applicant's arguments are not persuasive. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case Ueno discloses in the "Background of the invention" section, a copper seed layer 17, Fig. 1 or the like as a conductive layer is required [0006].

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571)- 272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yuriy Semenenko/
Examiner, Art Unit 2841

/Dean A. Reichard/
Supervisory Patent Examiner, Art Unit 2841